REMARKS

Claims 1, 3-9, 11-15, 17-25, and 28-30 are presented for further examination. Claims 1, 9, 13, 18-21, and 28 have been amended.

In the Office Action mailed December 19, 2005, the Examiner rejected claims 1, 3-7, 9, 11-15, 17-18, 20-25, and 28-30 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,883,846 ("Lee"). Claims 8 and 19 were found to be allowable if rewritten into independent form.

Applicants respectfully disagree with the basis for the rejection and request reconsideration and further examination of the claims.

For high speed operation of a memory device, it is necessary to sense the bit lines as soon as possible after the word line goes high and the bit line, which is connected to a low node, starts discharging. A sense amplifier is generally used for this purpose. The sensing branches of the sense amplifier are not symmetrical, as explained in the present application, due to tolerances in manufacturing process. This leads to an offset voltage inherent in the sense amplifier. To correctly sense the bit lines, it is required that the sense amplifier be enabled when the input voltage differences at the bit lines exceeds the offset voltage of the sense amplifier.

The foregoing high speed operation can be achieved in one of the two following ways:

1. The load on the bit lines can be reduced, thus enabling the bit line connected to the low node to discharge faster. This is the approach taken by the Lee patent.

Lee employs a negative feedback mechanism to connect inverter outputs of the sense amplifier with the bit lines. In Figure 4 of Lee, p105 connects SOUTB with DATA, and P106 connects SOUT with DATAB. After the sense amplifier is enabled, depending upon the state of the data latched, either of P105 and P106 will connect the "high" output of the sense amplifier with the "low" going bit line. The "low" going bit line stops going low any further. It

starts to charge instead. Thus, the sense amplifier shares the work of pre-charge devices (P112, P113, P121, and P122 in Figure 5), allowing them to be of a smaller size and hence presenting decreased load on bit lines.

2. The second approach is to reduce the asymmetry in the sense amplifier through some compensating means. This is the approach taken by the present invention.

In the discussed embodiments of the present invention, compensating means (170 and 180 in Figure 2 of the present invention) alter the resistance in the sensing branches of the sense amplifier for reducing the offset voltage. In addition, the circuit of the present invention delays the disconnection of the bit lines after the sense amplifier is enabled.

When reading the claims in their totality, it is clear that the approach taken by Lee is far different than that taken by the present claimed invention.

In claim 1, a sense amplifier for a memory array providing increased reliability and sensing small voltage differences is provided. The amplifier comprises two cross-coupled inverters forming a latch; supply coupling means for selectively connecting the latch to a supply source; compensating means for altering a resistance in sensing branches of the sense amplifier to correct an offset between the inverters of the latch; and bit line coupling means for selectively coupling inputs of each inverter to complementary bit lines from the memory array and delay means for delaying the disconnection of the bit lines from the sense amplifier after the latch has been coupled to a supply source.

In remarks accompanying the rejection, the Examiner states that Lee discloses "compensating means" as elements 102 and 103. While Lee at column 3, lines 50-55, uses the word "compensate" to imply that an input voltage difference of sufficiently high value should be applied to overcome an offset voltage. Lee describes the offset voltage as inherent to the sense amplifier due to a symmetry between the branch (101, 104, 102) and the branch (102, 106, 103). The reason being is that if an input voltage difference less than the offset voltage is applied, then the sense amplifier will latch a false state. Therefore, in order to latch a correct state by the sense

amplifier, a voltage difference of a value higher than the offset voltage (a voltage that compensates the offset voltage) must be applied.

In contrast, in the present invention elements 170 and 180 are the compensating means used to reduce the offset voltage because of asymmetry in the sense amplifier arising due to threshold voltage mismatch between elements 130 and 140. In the present invention, the compensating means alters the resistance in the sensing branches of the amplifier.

Furthermore, the bit line coupling means of claim 1 is not taught or disclosed in Lee. Lee uses NMOS (Figure 4, elements 102, 103) devices to couple DATA and DATAB with the sense amplifier. In particular, Lee describes connecting DATA and DATAB to the gate terminal of the NMOS elements 102, 103.

In contrast, the present invention utilizes PMOS elements (Figure 2, 150, 160) to couple the bit lines with the sense amplifier. The bit lines are connected to the drain terminal of the PMOS devices.

Claim 1 further recites delaying means. Lee does not teach or suggest a delaying means as claimed in the present invention. Rather, the description of Lee at column 3, lines 14-15 should be read along with the description at column 3, lines 6-13. **Here, by the word "delaying," Lee means the difference in time from Figure 6A (and 6B) to the time in Figure 6C**. After the word line and column line are opened (Figure 6A), and the control signals CDEQ in 20 and DTEQ in 40a go to logic high levels (Figure 6B), the enable signal (SAC) and the pre-charge signal (SEA) go to a logic high level after a predetermined time delay (*see* Figure 6C). With this, the pre-charge operation is completed and the sense amplifier starts sensing the voltage difference between DATA and DATAB. Thus, the "delay" referred to in Lee is the time difference between signals in one block (SAC and SEAQ in 10a, sense amplifier) and signals in other blocks (CDEQ in 20 and DTEQ in 40a, pre-charge circuits).

In contrast, the delaying of the present claimed invention implies the time when the enable signal (SAEN) goes high to the time when SAEND goes high to disconnect the bit lines from the sense amplifier. Note that this feature is unique to the present invention. First, the

sense amplifier is enabled, then after some delay the bit lines are disconnected from the sense amplifier. In Lee, the bit lines (DATA and DATAB) are always connected with the sense amplifier.

Moreover, at column 7, lines 27-30, which should be read in conjunction with column 7, lines 20-27, the word "delay" in Lee means that due to increased equalizing resistance of MP123 and MP124 there is a fast discharge of a low node of the bit line pair after the word line is selected. This reduces the delay time required in reaching the offset voltage. The "delay" here is the time from the word line going high (*see* Figure 6A), which causes the low node of the bit line pair to discharge quickly (Figure 6D), to the time when the voltage difference (at DATAA, DATAB) reaches the offset voltage (dV3, Figure 6D).

In contrast, in the present invention the "delaying means for delaying the disconnection of bit lines from the sense amplifier after the latch has been coupled to a supply source" is not disclosed, suggested, or claimed by Lee.

In view of the foregoing, applicants respectfully submit that claim 1 is clearly allowable over the teachings of Lee.

Dependent claims 3-8 are allowable for the features recited therein as well as for the reasons why claim 1 is allowable as well as for the features recited therein. For example, claim 4 recites the bit line coupling means to comprise a PMOS transistor. Lee's PMOS transistors 106, 105 are not bit line coupling means. They are negative feedback devices (*see* column 6, lines 44-48 and column 7, lines 19-21 read in conjunction with column 7, lines 4-18). Lee's elements 105 and 106 couple outputs of the sense amplifier SOUTB to DATA and SOUT to DATAB, thus providing negative feedback. In the present invention there is no negative feedback between the output of the sense amplifier and the bit lines. In addition, nowhere does Lee teach or suggest a pair of NMOS transistors that comprise a compensating means as recited in claim 5.

In addition, the delay is recited in claim 7 as being introduced between enabling of the supply coupling means and the bit lines. In contrast, the "delay" referred to by Lee is the

time interval from the word line going high (Figure 6A) to enable signal SAC going high (Figure 6C) after a sufficient voltage difference on bit lines is achieved to compensate offset voltage (dV3, Figure 6D). Lee reduces this delay time by increasing equalizing resistance of MP123 and MP124 as explained above. In the present claimed invention, the delay between enabling of the supply coupling means and disconnection of the bit lines is not taught, suggested, or claimed in Lee. In fact, Lee's bit lines are always connected with the sense amplifier as explained above.

Independent claim 9 is directed to a method for improving a latch-type sense amplifier for a memory array in order to increase reliability in sensing small voltage differences. The method includes cross-coupling two inverters to form a latch; selectively coupling the latch to a supply source; selectively coupling the inputs of each inverter to complementary bit lines from the memory array; delaying the disconnection of the bit lines from the sense amplifier until a predetermined duration after coupling the latch with the supply source; and altering a resistance in a sensing branch of the amplifier to correct an offset mismatch between the inverters of the latch. Applicants respectfully submit that claim 9 and dependent claims 11 and 12 are allowable for the reasons discussed above with respect to claim 1, *e.g.*, nowhere does Lee teach or suggest altering a resistance in a sensing branch of the amplifier to correct an offset mismatch between inverters of the latch.

Independent claims 13 and 18 recite the feature of altering a resistance in sensing branches of the amplifier as discussed above with respect to claims 1 and 9. Applicants respectfully submit that claims 13 and 18 and all claims depending therefrom are clearly allowable for the reasons discussed above with respect to claim 1. Independent claim 28 is allowable dependent claim 19 rewritten into independent format with claim 18. Applicants respectfully submit that claims 28-30 are allowable for the reasons why claim 19 is allowable.

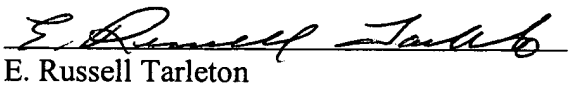
In view of the foregoing, applicants submit that all of the claims remaining in this application are now in condition for allowance. In the event the Examiner disagrees or finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative by telephone at (206) 622-4900 in order to

expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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